REMARKS

The specification is amended to clarify that the trenches of the invention have certain depths. Similar amendments are made to the claims. It is believed that these clarifying amendments do not introduce new matter into the application.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Parikh (U.S. Patent Number 6,225,207). Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu (U.S. Publication Number 2003/0001266). In view of the amended claims and the following remarks, it is believed that the claims are allowable over the cited references, and therefore, reconsideration of the rejections is requested.

The applicants' invention as claimed in amended independent claim 1 is directed to a method of manufacturing a semiconductor device having a first region and a second region. A first etching process is performed on an insulating layer formed on a semiconductor substrate, so that at least one first trench having a first depth and a second trench having the first depth are formed in the first region and the second region, respectively. A second etching process is performed on the second trench, so that a third trench having a second depth deeper than the first depth is formed in the second region. The insulating layer has a first thickness under the third trench and a second thickness under the at least one first trench. Specifically, the first thickness of the insulating layer under the third trench is less than the second thickness of the insulating layer under the at least one first trench. As a result, by increasing the second thickness of the insulating layer under the at least one first trench of the first region, wherein, in the first region, the capacitance of the insulating layer is the dominant cause of RC delay, the RC delay in the first region is minimized. In addition, as a result, by decreasing the first thickness of the insulating layer under the third trench of the second region, wherein, in the second region, the resistance of the insulating layer is the dominant cause of RC delay, the RC delay in the second region is minimized.

The applicants' invention as claimed in amended independent claim 5 is directed to a method of manufacturing a semiconductor device having a first region and a second region. A first etching process is performed using a first photoresist layer pattern as an etching mask, so

that a mask layer pattern, in which the first region and the second region are exposed, is formed. As a result of the first etching process, at least one first trench and a second trench having a first depth is formed in the first region and the second region, respectively. The first photoresist layer pattern is removed, and a second photoresist layer pattern, by which the at least one first trench of the first region is covered and by which the second trench and portions of the mask layer pattern are exposed is formed. A second etching process is performed using the second photoresist layer pattern and the mask layer pattern as an etching mask, so that a third trench having a second depth deeper than the first depth is formed in the second region. As a result, the insulating layer has a first thickness under the third trench and a second thickness under the at least one first trench. Specifically, the first thickness of the insulating layer under the third trench is less than the second thickness of the insulating layer under the at least one first trench. As a result, by increasing the second thickness of the insulating layer under the at least one first trench of the first region, wherein, in the first region, the capacitance of the insulating layer is the dominant cause of RC delay, the RC delay in the first region is minimized. In addition, by decreasing the first thickness of the insulating layer under the third trench of the second region, wherein, in the second region, the resistance of the insulating layer is the dominant cause of RC delay, the RC delay in the second region is minimized.

Independent claims 1 and 5 are amended to clarify certain features of the present invention. Specifically, claims 1 and 5 are amended to clarify the step of performing a second etching process, wherein an insulating layer has a first thickness under a third trench and a second thickness under at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under the at least one first trench. It is believed that these claim amendments clarify the patentable distinctions between the applicants' invention and the cited art.

Parikh fails to teach or suggest present invention, as set forth in the amended claims. Specifically, Parikh fails to teach or suggest performing a second etching process, wherein an insulating layer has a first thickness under a third trench and a second thickness under at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under the at least one first trench, as claimed. Instead, in

Parikh, a signal line trench pattern 332, referred to in the Office Action at page 3, paragraph 3 as a third trench, is etched to form a signal line trench 336 (see Parikh, Figures 3D-3E and column 7, lines 50-52). At the same time, in Parikh, a via hole 327, formed under signal line trench pattern 332, is extended by an etching process to form via hole 340, wherein via hole 340 extends from the signal line trench 336 to substrate 310 (see Parikh, Figure 3E and column 7, lines 53-57. There is no mention in Parikh of an insulating layer having a first thickness under a third trench, as claimed. Therefore, since Parikh fails to teach or suggest an insulating layer having a first thickness under a third trench, it follows that Parikh fails to teach or suggest a first thickness of the insulating layer that is less than a second thickness of the insulating layer under the at least one first trench, as claimed.

For these reasons, it is submitted that Parikh fails to teach or suggest these specific elements set forth in the amended claims. Therefore, reconsideration of the rejections of claims 1-8 under 35 U.S.C. 102(b) based on Parikh is respectfully requested.

Hu also fails to teach or suggest performing a second etching process, wherein an insulating layer has a first thickness under a third trench and a second thickness under at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under the at least one first trench, as claimed. Instead, in Hu, a pattern dielectric layer 110, referred to in the Office Action at page 4, paragraph 3 as an insulating layer, is patterned to define a via 114, referred to in the Office Action at page 4, paragraph 4 as a third trench, and trenches 112, wherein the via 114 has an etch depth that is greater than that of trenches 112 (see Hu, Figure 1A and page 3, paragraphs [0024]- [0025]). However, there is no mention that the via 114 of Hu is a third trench, which is formed so that the dielectric layer 110 has a first thickness under via 114, as set forth in the amended claims. Thus, it follows that Hu fails to teach or suggest an insulating layer having a first thickness under the third trench, as claimed. It further follows that Hu fails to teach or suggest a first thickness of the insulating layer that is less than a second thickness of the insulating layer, as claimed.

For these reasons, it is submitted that Hu fails to teach or suggest these specific elements set forth in the amended claims. Therefore, reconsideration of the rejections of claims 1-4 under 35 U.S.C. 102(e) based on Hu is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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